REMARKS

Claims 12-20, 35, and 36 are present in the application.

New claims 35 and 36 have been added. Support for the new claims can be found throughout the specification and the claims as originally filed, and particularly in paragraphs [0068]-[0083] and Figures 6-16.

Claim 12 has been amended to be dependent on claim 35.

No new subject matter has been added.

Claim Rejections – 35 USC 103

Claims 12-20 are rejected for being obvious having regard to Balakrishnan in view of Tan and Hamamoto.

New independent claim 35 recites a data transmitter comprising "a signal transmitter for sending each one of the plurality of first and second output signals on a respective one of substantially parallel conductors of a bus" and a "delay generator for delaying said second output signals by a delay period T_DLY relative to said first output signals", "wherein the clock period T_CLK is greater than the delay period T_DLY".

The Applicant respectfully submits that at least these elements are not taught or suggested by the cited references, taken alone or in combination.

Balakrishnan teaches a system for reducing skew in the parallel transmission of digital data slices (abstract). Balakrishnan teaches controlling clock signals to reduce skew when a clock signal is routed to multiple devices. As described at column 2, lines 5-8, the objective of the system taught by Balakrishnan is to reduce the skew effects between parallel data slice paths, i.e. reducing a delay period between the parallel data slice paths. Clearly, it cannot be said that Balakrishnan teaches a system comprising a "delay generator for delaying said second output signals by a delay period T_DLY relative to said first output signals", as recited in claim 35.

Hamamoto teaches a chip for a synchronous dynamic random access memory (SDRAM) with self-skew compensation. As described in section B entitled "Self-Skew

Compensation Technique" found at pages 771-773, the purpose of Hamamoto is to reduce the delay period between signals, which is contrary to what is being recited in claim 35. Therefore, it cannot be said that Hamamoto would teach or suggest the delay generator recited in claim 35.

Tan teaches a device for routing dynamic signals and static signals. The signal line routing scheme taught by Tan includes a plurality of dynamic signal lines disposed in parallel to each other, and a plurality of static signal lines disposed in parallel to each other and also disposed in parallel with the plurality of dynamic signal lines, wherein at least one of the plurality of static signal lines is disposed immediately adjacent to each one of the plurality of dynamic signal lines.

Tan teaches two different types of signals, static (source controlled) and dynamic (multi-pull-down-bus) signals. According to Tan, there are two types of static signals: first static signals that change during precharge (see Fig. 2B) and second static signals that change during evaluation. The second static signals can coincidentally change at the same time as a dynamic line. In this case, Tan teaches to add a delay to the second static signals or the dynamic signals (col.4, lines 64 to col.5, line 4).

The Applicant submits that the skilled person would understand that only the dynamic signals taught by Tan are bus signals. The static signals are not part of the bus. The static signals are used for driving and latching a bus which outputs the dynamic signals (col. 4, lines 5-8). At col. 4, lines 5-14, Tan teaches that the static signals may not change at the same time as the dynamic bus. This can only occur if the static signals are not bus signals.

However, Tan does not teach or suggest adding a delay between the bus signals, i.e. the dynamic signals, but only between the static signals and the dynamic signals. Therefore, it cannot be said that Tan would teach or suggest "a signal transmitter for sending each one of the plurality of first and second output signals on a respective one of substantially parallel conductors of a bus" and "a delay generator for delaying said second output signals by a delay period T_DLY relative to said first output signals", as recited in claim 25.

Furthermore, Tan is silent about the value of the delay to be added between the static signals and the dynamic signals. Therefore, it cannot be said that Tan would teach or suggest that "the clock period T_CLK is greater than the delay period T_DLY", as recited in claim 35.

Therefore, the Applicant respectfully submits that the cited references, taken alone or in combination, fail to teach or suggest all of the elements of claim 35.

Furthermore, the Applicant respectfully submits that both Balakrishnan and Hamamoto teach away from a "delay generator for delaying said second output signals by a delay period T_DLY relative to said first output signals" as recited in claim 35 since the objective of these references is the reduction of a delay period between signals.

At page 3 of the Office Action dated May 12, 2020, the Examiner asserts that Tan is in the same field of endeavor as Balakrishnan. The Applicant respectfully disagrees with the Examiner. While the objective of Balakrishnan and Hamamoto is to reduce the time variations between signals, the objective of Tan is to eliminate crosstalk between adjacent dynamic lines, i.e. to eliminate amplitude variations on each dynamic signal (see Tan, col. 2, lines 61-67). The Applicant respectfully submits that reducing time variations between signals and reducing signal variation amplitude are not in the same field of endeavor, and therefore, the skilled person would not combine Balakrishnan and Hamamoto which are about time variations between signals with Tan which teaches a device for reducing amplitude variations. The Applicant submits that the combination of the cited reference is therefore improper.

In view of the arguments provided above, the Applicant submits that claim 35 is compliant with 35 USC 103.

Claims 12-20 and 36 are also believed to be compliant with 35 USC 103 at least because they depend on claim 35.

Conclusions

Claims 12 to 20, 35, and 36 are said to be allowable over the cited prior art and a Notice of Allowance is earnestly solicited.

Respectfully submitted,

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